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Brick Layer Model Analysis of Nanoscale-to-Microscale Cerium Dioxide

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Abstract. The frequency-dependent impedance/dielectric behavior of the brick-layer model (BLM) was investigated vs. grain size and local parameters (resistivity, dielectric constant, and grain boundary width). The simulation shows a maximum in capacitance vs. grain size, governed by the grain boundary-to-grain interior resistivity ratio. The BLM was employed to analyze the 500 °C impedance behavior of polycrystalline cerium dioxide from the nano- (~ 15 nm grain size) to the micro- ($\sim 4\,\mu$m grain size) regime. The grain boundary resistivity is orders of magnitude larger than that of the grain interiors in the microcystalline specimen. This contrast is significantly smaller in the nanocrystalline specimens, suggesting enhanced conduction at grain boundaries. The limitations of the BLM for simulating the behavior of complex electroceramic microstructures are discussed.

Keywords: nanocrystals, cerium oxide, grain boundaries, dielectric constant, brick layer model

Introduction

It is a well-established fact that many electroceramics exhibit grain boundary-controlled behavior. Bauerle [1] is credited with the development of an equivalent circuit model for conductive ceramics with resistive grain boundaries. Beekmans and Heyne [2] reported microstructures (i.e., second phase grain boundary layers) and the corresponding frequency-dependent impedance behavior consistent with these impediments to overall transport. Their rough model was further quantified by van Dijk and Burgraaf [3], in what came to be known as the ''brick layer model'' [4], hereafter referred to as the BLM. This model is routinely employed to describe the frequency-dependent electrical behavior of polycrystalline electroceramics, including ionic conductors [5] and electronic conductors [6]. The latter category includes the well-known and technologically important grain boundary electroceramics, e.g., varistors, positive temperature coefficient of resistance (PTCR) thermistors, and grain boundary layer capacitors [6]. More recently, Maier [7] and Näfe [8] have taken into account the parallel grain boundary contributions in materials with conductive grain boundaries.

The BLM can be understood with the aid of Fig. 1. A 3-D array of monosized cubic grains (''bricks'') is constructed with uniform grain boundary layers (''mortar'') separating them. A single grain and its surrounding grain boundary layers are represented in the figure. (Note that only half of each grain boundary belongs to a given grain.) If the grain boundary conductivity (σ_{gb}) is much smaller than that of the grain interiors (σ_{gi}), as is often the case in electroceramics, and the grain boundary width is negligibly small vis-à-vis the grain size, e.g., nm vs. μm, then for an electric field applied in the vertical direction the contributions of the *parallel* grain boundaries (the ''parallel path'' in Fig. 1(b)) can be neglected. Transport is dominated by the *series* path (top and bottom grain boundary layers and the grain cores), resulting in a Bauerle-type equivalent circuit consisting of two parallel RC (resistor-capacitor) networks, one for the grains and one for the grain

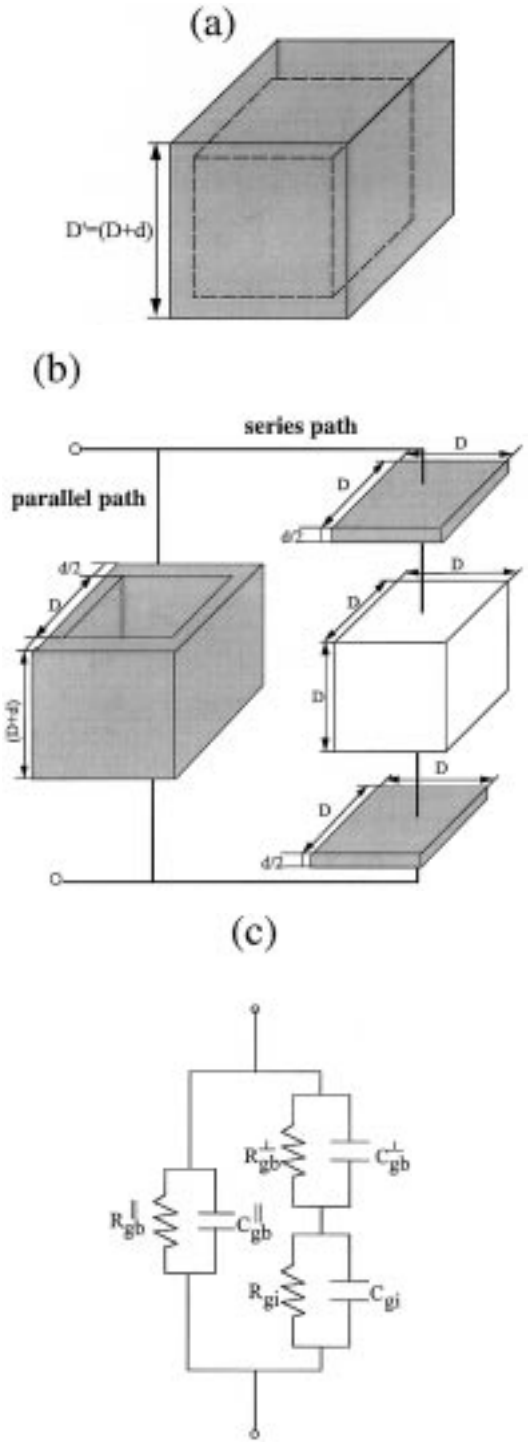

Fig. 1. Schematic representation of the brick layer model (BLM). (a) A representative unit of the BLM. (b) Separation of grain interior and grain boundary components. (c) the equivalent circuit. (D' denotes the apparent grain size, the sum of grain interior size, D, and grain boundary width, d.)

boundaries, connected in series. The capacitance ratio of the two components is:

$$\frac{C_{gb}}{C_{gi}} = \frac{\varepsilon_{gb}}{\varepsilon_{gi}} \frac{D}{d} \tag{1}$$

where C_{gb} and C_{gi} are the effective capacitances of the sample attributable to each component, ε_{gb} and ε_{gi} are the grain boundary and grain interior dielectric constants, D is grain interior size and d is grain boundary width. D' is the apparent grain size ($D' = D + d$). (see Fig. 1) This simplified BLM appears to work quite well as long as the assumptions made, i.e., $\sigma_{gb} << \sigma_{gi}$ and $d << D$, are reasonable.

Näfe [8] pointed out the necessity of taking the *parallel* grain boundary contributions into account when the grain boundary conductivity becomes significantly larger than that of the grain interiors. This can occur in microcrystalline (grain size $\geq \mu$m) ceramics when the conductivity ratio, σ_{gb}/σ_{gi}, is large enough to compensate for the small fraction of grain boundary material. Näfe [8] extended the simplified BLM and showed how parallel grain boundary conduction contributed to the overall ionic conductivity of solid electrolytes. His treatment dealt with conductivity exclusively; dielectric properties were not considered.

Even if σ_{gb}/σ_{gi} is small, it is reasonable to expect the simplified BLM to fail when the grain boundary width (d) is no longer negligible compared to the grain size (D), i.e., in nanophase ceramics. Under these conditions the contribution of the parallel grain boundaries to the dielectric constant is not negligible, as we will show. The complete BLM solution must be considered to successfully model the dielectric behavior.

In spite of the recent development and extensive study of nanophase ceramics, the electrical/dielectric properties have not received adequate attention. Lee et al. [9] reported a primitive varistor-like grain boundary behavior in nanophase ZnO, based upon impedance measurements under dc bias. Mo et al. [10] observed enhanced dielectric constants in nanocrystalline TiO_2, Al_2O_3, and amorphous Si_3N_4 and attributed these to the increased interfaces in their materials. Chiang et al. [11] performed impedance measurements on densified nanocrystalline CeO_2 and observed distinct grain boundary and grain interior arcs. They also made careful comparisons with coarsened microcrystalline ceria insofar as electrical

conductivity was concerned. Their conclusion was that nanocrystalline ceria possesses greatly reduced grain boundary impedance and increased electronic conductivity, corresponding to a heat of reduction that is less that one-half its value in single crystals and microcrystalline samples. We recently reported similar findings for pressureless-sintered, porous nanophase ceria with ~ 15 nm grain size [12].

None of the nanophase ceramic studies to date have focused on the dielectric properties. In particular, it is possible to cover the entire range from nanoscale to microscale by sintering at progressively higher temperatures for fixed times or with longer times at a fixed sintering temperature. We employed the former procedure in the present study. The goal of this study was to investigate the frequency-dependent behavior of the BLM, based on the grain boundary vs. grain interior properties (resistivities, dielectric constants, grain boundary width, and grain size) and to determine whether the impedance/dielectric behavior of polycrystalline (nano- to microcrystalline) cerium dioxide is consistent with the BLM.

Experimental

The complex impedance response of the BLM structure was modeled using the geometric configuration shown in Fig. 1. The RC elements in the series path were assumed to be in parallel with the RC element of the parallel path. The electrical/dielectric response is determined by six parameters, D (grain size), d (grain boundary width), the two resistivities (ρ_{gb} and ρ_{gi}) and the two dielectric constants (ε_{gb} and ε_{gi}), where $gb =$ grain boundary and $gi =$ grain interior. Given the material of interest (ceria) and to simplify the parameter matrix, both dielectric constants were assumed to be 30. [13] Nyquist and bode plots were generated vs. grain size using the equations described below.

Nanocrystalline cerium oxide powder prepared by the inert gas condensation route (Nanophase Technologies Corp., Burr Ridge, IL) and having an initial particle size of 5 nm was pressed at 125 MPa into pellets approximately 20 mm in diameter by 2 mm in thickness. These pellets were then subjected to cold isostatic pressing at 280 MPa. Each pellet was dried at 200 °C for 2 h to eliminate the water adsorbed and subsequently heated (at 2 °C/min) to 700, 800, 900, 1000, or 1100 °C, where it was held for 1 h. After sintering, the samples were cooled at 2 °C/min to 430 °C and subsequently furnace-cooled to room temperature for impedance, grain size, and density measurements. The impedance pellets were polished with 600 grit SiC abrasive paper, followed by sequential wheel polishing with 30, 6, and 1 μm diamond pastes. The polished surfaces were coated with 0.15 μm thick gold electrodes by sputtering. Our prior work suggested that improper electroding, i.e., using pressed foils alone or insufficiently thick sputtered electrodes, can lead to artifacts in the impedance spectra [14]. In the present work, 4-point dc resistance measurements on bar specimens cut from identically prepared pellets were employed to confirm that the features obtained were attributable to the specimen and not to spreading resistance at imperfect electrodes.

Impedance measurements were conducted in a muffle furnace at 500 °C in air, using a spring-loaded alumina specimen holder. Extreme care was taken to use separate grounded shields for each wire leading to the sample, in order to reduce apparatus contributions to the overall impedance spectra [15]. In addition, the acquired spectra were corrected for any residual apparatus contributions using standard open- and closed-circuit null corrections [16]. The impedance analyzer was an HP-4192A (Hewlett-Packard, Palo Alto, CA) operating with an oscillating voltage of 1V over the frequency range of 13 MHz to 5 Hz, with 20 points per decade.

Phase identification was confirmed using X-ray diffraction (XDS 2000, Scintag, Santa Clara, CA). The grain sizes were determined on micrographs of fracture surfaces using a high resolution field-emission scanning electron microscope (S-4500, Hitachi, Tokyo, Japan). At least 50 grains were measured for each specimen. Sample densities were determined using the Archimedes method, except for the as-compacted samples, whose measured dimensions and weights were employed.

Results and Discussion

A. Experimental Results

X-ray diffraction patterns for the as-compacted and sintered materials showed peaks corresponding to cerium oxide only. As expected, there was particle-

Table 1. Post-sintering densities

Sintering temperature [°C]	Percent theoretical density
As-compacted	~ 42*
700	67
800	69
900	75
1000	97
1100	94

*Average of 3 samples.

size broadening in the patterns of the unsintered and poorly-sintered (700 °C, 800 °C) specimens. As we reported previously [12], the starting material employed was found to contain 8–10 wt% of tungsten (by spark source mass spectrometry), apparently present as insoluble oxide precipitates at an overall atom fraction too small to be detected above background in our X-ray patterns. Chiang et al. [11] concluded that these second-phase particles are inert with respect to ceria, since the defect behavior is unaffected vis-à-vis pure samples made by other means. Our prior results [12] are consistent with this interpretation.

As-compacted pellet densities were approximately 42%, as shown in Table 1. Also shown are the densities after sintering at each temperature. As expected, densities increase with sintering temperature, approaching theoretical density above 1000 °C. The corresponding grain sizes as determined by scanning electron microscopy are given in Fig. 2. The error bars indicate the standard deviation of at least 50 individual measurements for each specimen. Grain size remains small, 15–20 nm, after sintering at 700 °C and 800 °C, consistent with the line broadening in the X-ray patterns. At higher temperatures, grain size grows to ~ 100 nm between 900° and 1000 °C, and into the micron range by 1100 °C.

Nyquist plots of -imaginary vs. real impedance are shown in Fig. 3(a), with an enlargement of the high frequency (leftmost) portion of each spectrum given in Fig. 3(b). A large and distinct low frequency (rightmost) arc is only apparent for the 1100 °C-sintered (microcrystalline) specimen. In comparison, the 700 °C-sintered (~ 15 nm) sample exhibits what appears to be a single arc which is centered on the real axis. For samples sintered at intermediate temperatures a distorted arc is obtained, as evidenced by depression of the arc center below the real axis, or some indication of an additional component appearing at low (rightmost) frequencies, e.g., in the 800 °C-sintered sample spectrum. Although it was possible to fit these spectra with two separate arcs, each arc was significantly depressed below the real axis. In such cases the constant phase element (CPE) parameters obtained by fitting, are not reliable indicators of the dielectric behavior [17].

B. Simulation

Based on the equivalent circuit of Fig. 1(c), the measured impedance, Z_m, and the individual grain interior and grain boundary contributions (Z_{gi}, $Z_{gb}^{\parallel}$, and $Z_{gb}^{\perp}$) contributions are given

$$Z_m = \frac{1}{\left[\frac{1}{Z_{gb}^{\parallel}} + \left(\frac{1}{Z_{gb}^{\perp} + Z_{gi}}\right)\right]} \tag{2}$$

$$Z_{gi} = \frac{1}{\left[\frac{1}{\rho_{gi}}\frac{D^2}{D} + j\omega\varepsilon_o\varepsilon_{gi}\frac{D^2}{D}\right]} \tag{3}$$

$$Z_{gb}^{\parallel} = \frac{1}{\left\{\frac{1}{\rho_{gb}}\frac{[(D+d)^2 - D^2)]}{(D+d)} + j\omega\varepsilon_o\varepsilon_{gbi}\frac{[(D+d)^2 - D^2)]}{(D+d)}\right\}} \tag{4}$$

$$Z_{gb}^{\perp} = \frac{1}{\left[\frac{1}{\rho_{gb}}\frac{D^2}{d} + j\omega\varepsilon_o\varepsilon_{gb}\frac{D^2}{d}\right]} \tag{5}$$

Here angular frequnecy, ω, is related to the frequency, f, by $\omega = 2\pi f$. The impedance is transformed into real capacitance vs. frequency

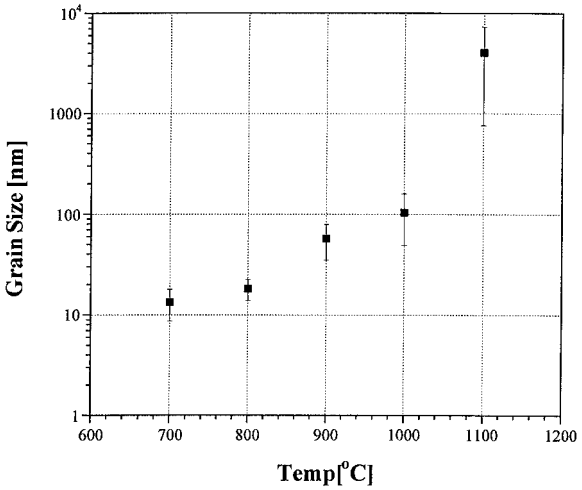

Fig. 2. Grain size, as determined by scanning electron microscopy, of nanophase cerium oxide sintered between 700 °C and 1100 °C (1 h treatments). The error bars represent the standard deviation on 50 + individual grains.

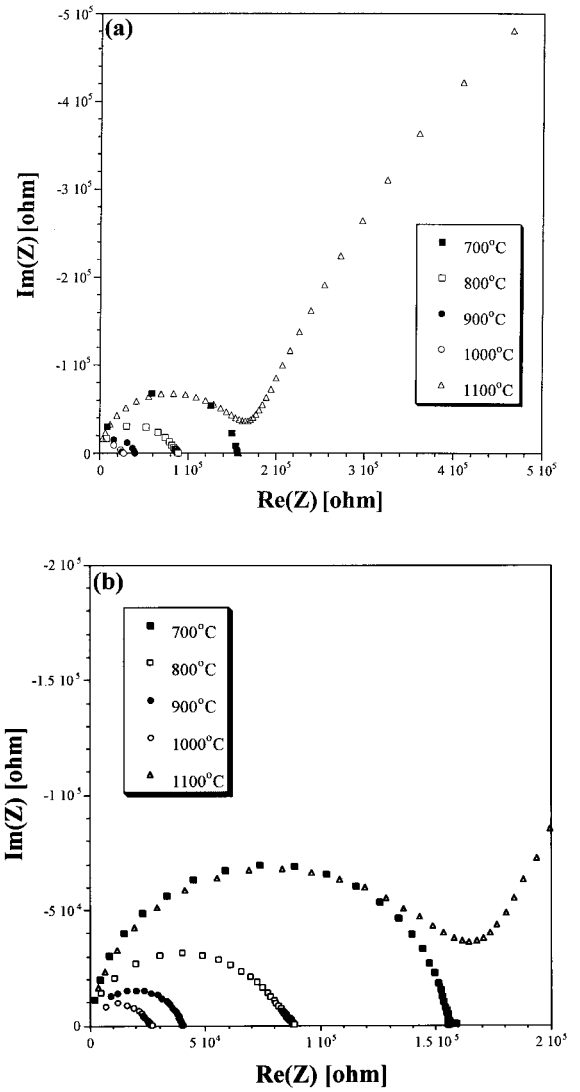

Fig. 3. (a) Post-sintering impedance spectra (measured at 500 °C in air) of specimens sintered between 700 °C and 1100 °C (1 h treatments). (b) Enlargement of the high frequency region of the impedance spectra.

using the following complex transformation

$$C_{re} = \mathrm{Re}\left[\frac{1}{j\omega}\frac{1}{Z_m}\right] = \mathrm{Re}\left[\frac{1}{j2\pi f}\frac{1}{Z_m}\right] \qquad (6)$$

Figure 4 shows Nyquist and Bode plots (Z_m vs. frequency, C(real) vs. frequency) for a simulation where the microstructural aspect ratio (D/d) is significantly less than the grain boundary-to-grain interior resistivity ratio, ρ_{gb}/ρ_{gi}, which was fixed at 10^3. This situation is typical of grain boundary-controlled electroceramics, with the grain boundary (rightmost) arc being much larger than the grain interior (leftmost) arc on the Nyquist plot. Two plateaus are apparent in each Bode plot.

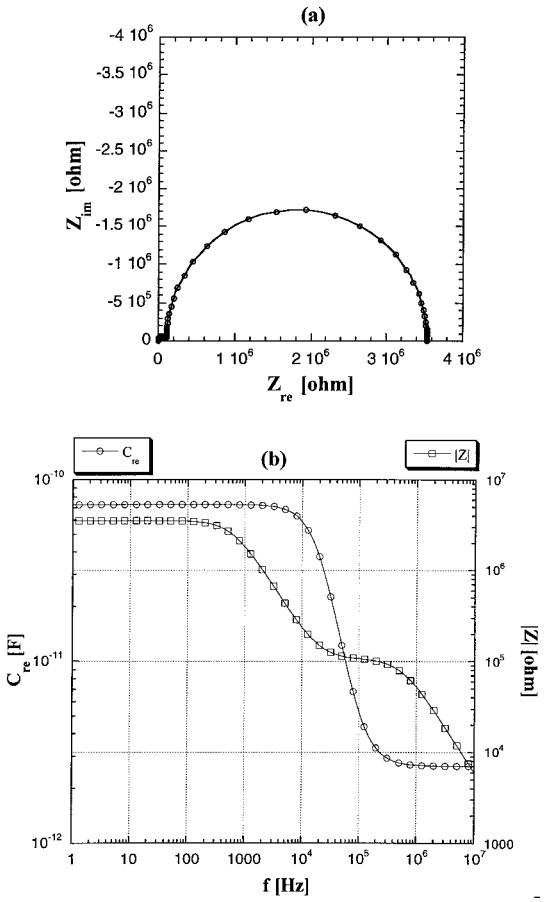

Fig. 4. Impedance simulations for a condition where $D/d < \rho_{gb}/\rho_{gi}$ ($\rho_{gb}/\rho_{gi} = 10^3$, $\varepsilon_{gb} = \varepsilon_{gi} = 30$, $D/d = 30$) (a) Nyquist plot and (b) the corresponding capacitance and impedance Bode plots (C_{re} = real capacitance).

In contrast, Fig. 5 shows Nyquist and Bode plots for a situation where D/d is much greater than ρ_{gb}/ρ_{gi}. Now the grain boundary arc is a barely discernable feature on the right (low frequency) side of the dominant grain interior arc. Note that whereas two plateaus are still apparent in the capacitance Bode plot, the grain boundary (low frequency) plateau in the impedance Bode plot is virtually absent.

Figure 6 plots the ratio of the two capacitance Bode plateau values, $C(lof)/C(hif)$, vs. the microstructural aspect ratio, D/d, for the situation where the grain boundary-to-grain interior resistivity ratio (ρ_{gb}/ρ_{gi}) is 10^3. Note the positions of the prior simulations, i.e.,

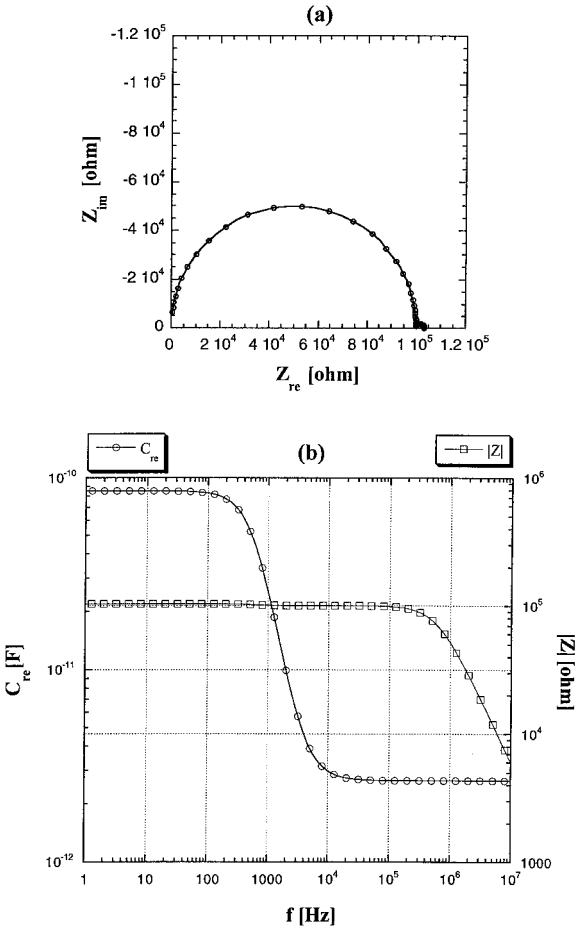

Fig. 5. Impedance simulations for a condition where $D/d > \rho_{gb}/\rho_{gi}$. ($\rho_{gb}/\rho_{gi} = 10^3$, $\varepsilon_{gb} = \varepsilon_{gi} = 30$, $D/d = 3 \times 10^4$) (a) Nyquist plot and (b) the corresponding capacitance and impedance Bode plots (C_{re} = real capacitance).

$D/d < \rho_{gb}/\rho_{gi}$ (marked ''A'', corresponding to Fig. 4) and $D/d > \rho_{gb}/\rho_{gi}$ (marked ''B'', corresponding to Fig. 5). In the two limits of Fig. 6, where there are no grain cores $(D/d \to 0)$ or no grain boundaries $(D/d \to \infty)$, the system is homogeneous and there is no enhancement of capacitance above the high frequency, $C = \varepsilon_r \varepsilon_o$ (A/l), value (where A and l are sample area and length, respectively, ε_o is the permittivity of free space, and the relative dielectric constant, $\varepsilon_r = 30$). However, as grain size is increased from zero, the low frequency (grain boundary-derived) capacitance increases linearly with grain size (e.g., in the vicinity of point ''A'' in Fig. 6). This is consistent with the traditional BLM Eq. (1). Eventually, the special situation is reached where $D/d \sim \rho_{gb}/\rho_{gi}$. The Nyquist and Bode plots of Fig. 7

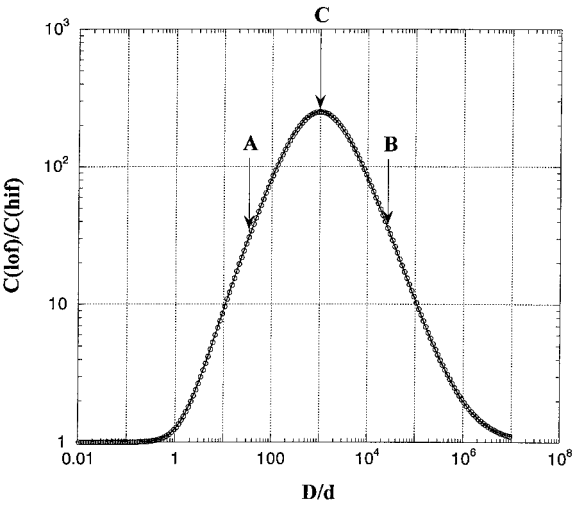

Fig. 6. Capacitance ratio $[C(lof)/C(hif)]$ vs. microstructural aspect ratio (D/d). ($\rho_{gb}/\rho_{gi} = 10^3$, $\varepsilon_{gb} = \varepsilon_{gi} = 30$.)

show that in this condition the grain interior and series grain boundary resistances are identical; their Nyquist arcs are the same size. There are two plateaus in each Bode plot. The low frequency-to-high frequency capacitance ratio, $C(lof)/C(hif)$, has its maximum value here (corresponding to point ''C'' in Fig. 6). The subsequent drop in capacitance with increasing grain size can be understood with the help of Fig. 1. Beyond the maximum, the series resistance due to grain boundaries $(R_{gb}^{\perp})$ becomes much smaller than the resistance due to the grain interiors (R_{gi}), effectively shorting-out the large $(C_{gb}^{\perp})$. Situation ''B'' lies in this regime.

It should be also pointed out that Fig. 6 is not symmetrical about its maximum value. This is due, in part, to the increasingly important role of parallel grain boundary contributions at the smallest grain sizes ($R_{gb}^{\parallel}$ in Fig. 1). In the nanoscale regime, the substantial volume fraction of grain boundary material can be expected to play an important role.

We also investigated, via simulation, the effect of individual parameters, e.g., grain boundary resistivity and grain boundary dielectric constant, on the impedance/dielectric response. The results are displayed in Figs. 8(a) and (b). Figure 8(a) shows that $C(lof)/C(hif)$ increases with ρ_{gb}/ρ_{gi}. (Here we hold $\varepsilon_{gb} = \varepsilon_{gi} = 30$ and $d =$ constant.) This may explain why such a maximum in capacitance vs. grain size is not usually observed. At a value of $\rho_{gb}/\rho_{gi} = 10^6$ and a reasonable grain boundary width (e.g., 10 nm), this maximum would be reached at a grain size of 10 mm.

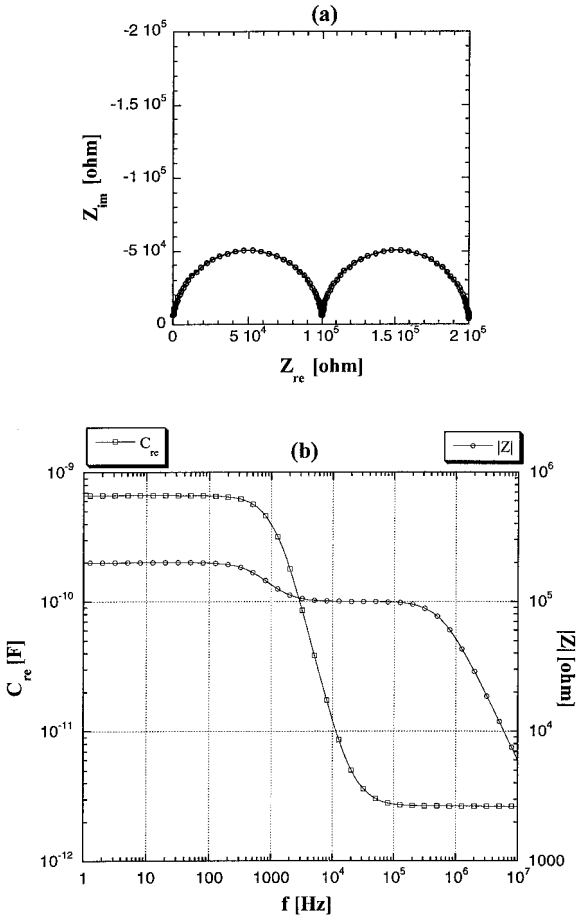

Fig. 7. Impedance simulations for a condition where $D/d \sim \rho_{gb}/\rho_{gi}$. ($\rho_{gb}/\rho_{gi} = 10^3$, $\varepsilon_{gb} = \varepsilon_{gi} = 30$, $D/d = 1 \times 10^3$) (a) Nyquist plot and (b) the corresponding capacitance and impedance Bode plots (C_{re} = real capacitance).

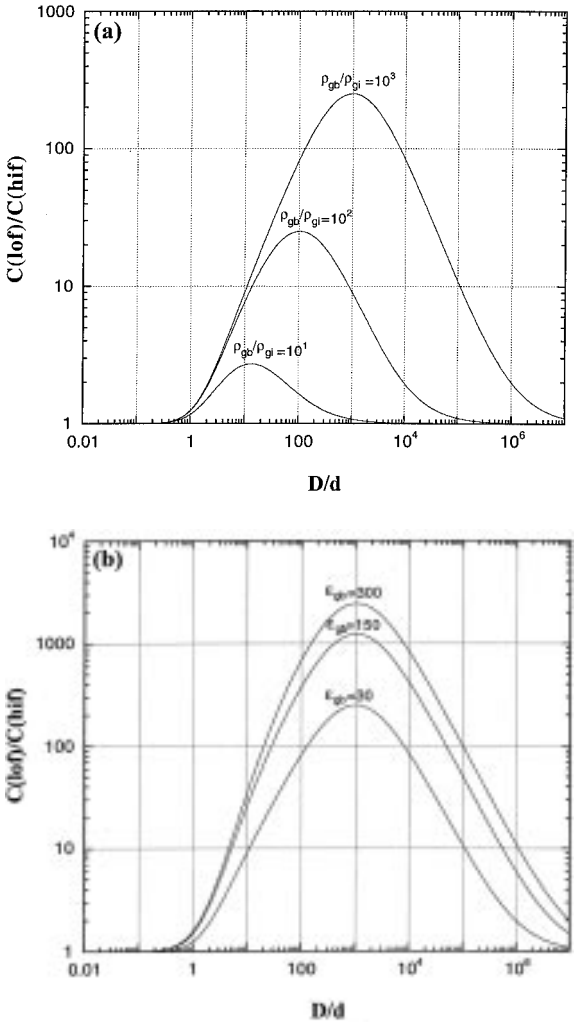

Fig. 8. (a) Effect of local resistivity (of grain boundaries) on the capacitance ratio, $C(lof)/C(hif)$, as a function of microstructural aspect ratio (D/d), assuming that $\varepsilon_{gb} = \varepsilon_{gi} = 30$. (b) Effect of local dielectric constant (of grain boundaries) on the capacitance ratio, $C(lof)/C(hif)$, as a function of microstructural aspect ratio (D/d), assuming that $\rho_{gb}/\rho_{gi} = 10^3$.

Most conventional microcrystalline electroceramics possess similarly large values of ρ_{gb}/ρ_{gi}, however with grain sizes in the μm rather than the mm range. In Fig. 8(b) we hold $\rho_{gb}/\rho_{gi} = 10^3$ and $\varepsilon_{gi} = 30$, but now vary the grain boundary dielectric constant. Although the capacitance increases at every frequency, the position of the maximum does not shift. The D/d corresponding to the maximum capacitance is strictly governed by the grain boundary-to-grain interior resistivity ratio in the BLM.

C. BLM Analysis of Nano-to-Microcrystalline Ceria

Figures 9(a) and (b) display the 500 °C experimental data in Bode format for nanophase ceria sintered at progressively higher temperatures (and to successively larger grain sizes) as described above. For the purpose of comparison, the capacitance values (Fig. 9(a)) are shown as a function of frequency. As can be seen, except for the 700 °C-sintered specimen, which has a relatively flat capacitance vs. frequency behavior, the other samples displayed dual-plateau capacitance behavior. (The data below 500 Hz were quite noisy and are not shown.) On the other hand, only the 1100 °C-sintered (microcrystalline) specimen showed dual plateaus in the impedance Bode plots

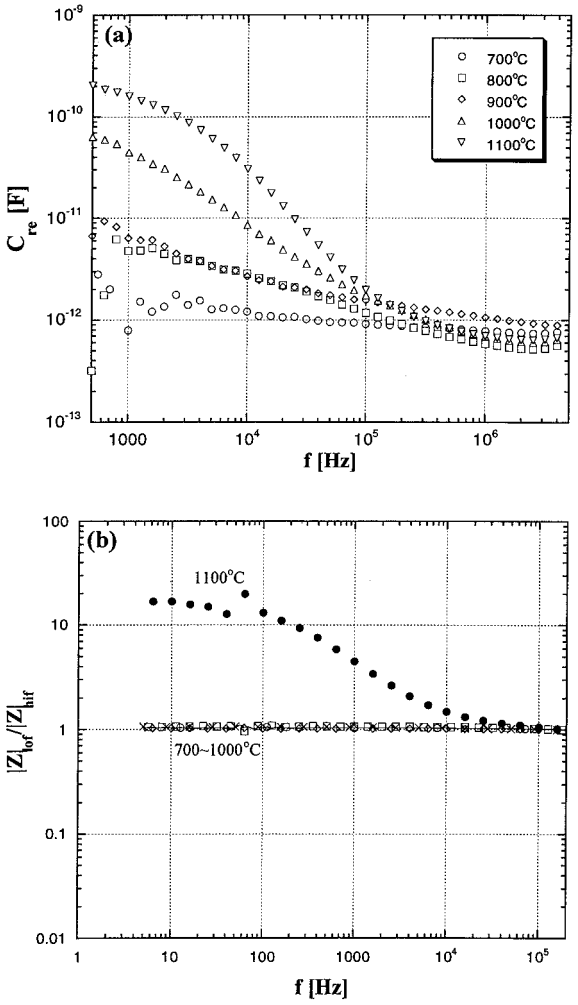

Fig. 9. (a) Capacitance (based upon overall specimen geometry) vs. frequency, and (b) Normalized impedance vs. frequency (measured at 500 °C in air of specimens sintered between 700 °C and 1100 °C for 1 h).

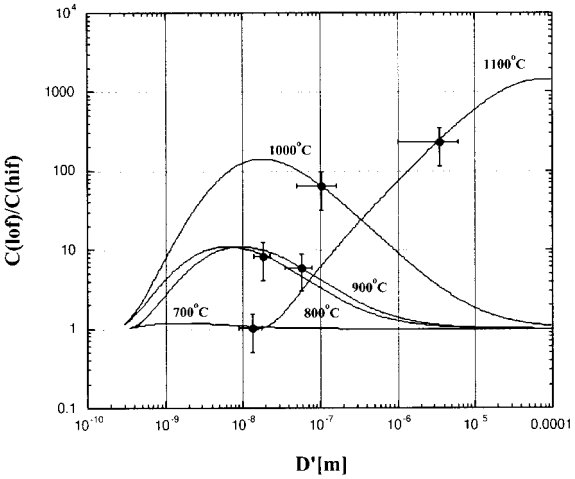

Fig. 10. Comparison of experimental and brick layer model (BLM)-predicted $C(lof)/C(hif)$ using the parameters in Table 2. (The horizontal error bars represent the standard deviation on 50 + individual grains, the vertical error bars represent a factor of 2 uncertainty in the measured capacitance.)

(Fig. 9(b)). Assuming the BLM to be applicable, only the microcrystalline (1100 °C) specimen would be to the left of the maximum in Fig. 6 (i.e., situation ''A'' with Bode plots like Fig. 4). All the nanocrystalline samples behave as if to the right of the maximum in Fig. 6 (i.e., situation ''B'' with Bode plots like Fig. 5). In other words, the resistivity ratio, ρ_{gb}/ρ_{gi}, is large for the microcrystalline specimen, but much smaller for the nanocrystalline specimens. This places severe constraints on allowable modeling parameters with the BLM approach, as we now discuss.

Figure 10 shows experimental $C(lof)/C(hif)$ vs. grain size together with simulated $C(lof)/C(hif)$ vs. grain size using the BLM. As discussed above, only the microcrystalline (1100 °C) simulation places the experimental datum to the left of the capacitance maximum, as shown. The simulated Bode plots (not shown) behaved as in Fig. 4 and displayed dual plateaus in both Bode plots, as seen experimentally (Fig. 9). Each of the nanocrystalline simulations places the experimental datum to the right of the capacitance maximum in Fig. 10. The simulated Bode plots (not shown) behaved as in Fig. 5, with dual plateaus in capacitance vs. frequency, but a single plateau in impedance vs. frequency, as seen experimentally (Fig. 9). This demonstrates that the BLM is capable of generating the impedance/dielectric features observed in both nanocrystalline and microcrystalline ceria. The parameters employed in each of these simulations are given in Table 2.

Table 2. Brick layer model parameters used in fitting the experimental results in Fig. 10

T [°C]	ρ_{gb} [ohm^{-1} cm^{-1}]	ρ_{gi} [ohm^{-1} cm^{-1}]	ε_{gb}	ε_{gi}	d [nm]
700	3×10^{4}	3×10^{4}	200	30	0.25
800	2×10^{5}	3×10^{4}	900	30	0.2
900	2×10^{5}	3×10^{4}	900	30	0.3
1000	1.5×10^{5}	4×10^{3}	900	30	0.2
1100	1.1×10^{8}	2×10^{4}	30	30	13

Whereas the grain boundary resistivity of the microcrystalline 1100 °C specimen is much larger than that of the grain interiors ($\sim 10^8$ vs. $\sim 10^4\,\Omega$-cm), this contrast is decidedly smaller for the nanocrystalline specimens ($\sim 10^4$ to 10^5 vs. $\sim 10^4\,\Omega$-cm). This is also clear from the experimental results (i.e., no distinct grain boundary Nyquist arc or low frequency plateau in impedance Bode plots for the nanocrystalline specimens). The enhancement of conductivity at grain boundaries is consistent with prior dc conductivity results in nanophase ceria by ourselves and Chiang et al. [11,12].

Although the BLM can successfully account for the various impedance/capacitance features obtained for nano- to microcrystalline ceria, the underlying simulation parameters are problematic. While it was possible to obtain BLM fits comparable to those reported in Fig. 10 and Table 2, unrealistically small (sub-nanometer) grain boundary widths were required. Although it was possible to fit the data with larger ($\geq$ nm) grain boundary widths, unrealistically large grain boundary dielectric constants $(\varepsilon_{gb} > 10^3)$ were required. As it stands, the grain boundary dielectric constants are inexplicably large.

There are a number of reasons why the BLM may not be valid or applicable to the present situation. First, the specimens in the present study were not completely dense (see Table 1). There are legitimate concerns that the BLM is not an appropriate representative for ''real'' microstructures of dense polycrystalline ceramics. For example, Anderson and Ling [18] performed computer simulations for thin films using actual grain topologies which showed significant disagreement with BLM predictions insofar as dc conductivity was concerned. The extensive porosity and unusual grain-to-grain connectivity in the present study compounds the situation. Second, the BLM assumes a discrete grain boundary thickness, and we have assumed that this does not change with grain size in Fig. 10. In fact, the grain boundary thickness is rather less clearly defined, e.g., in the instance of a space charge layer. Furthermore, it is very likely to vary with grain size, as demonstrated by Terwillinger and Chiang [19] in the instance of a grain size-dependent segregation of impurities to grain boundaries. This could result in both grain boundary width and dielectric constant varying with grain size. Finally, the BLM ignores any distribution of grain interior sizes/properties and/or in grain boundary widths/properties. Such distributions are believed to play an important role in governing the properties of microcrystalline electroceramics [20].

Conclusions

Impedance measurements at 500 °C and grain growth studies were performed on nanophase cerium oxide compacted and sintered at temperatures from 700 °C to 1100 °C, to grow the grains from the nanometer to the micrometer range. Dual-plateau behavior, typical of grain boundary-controlled electroceramics, was observed in capacitance Bode plots for all specimens except the 700 °C-sintered specimen with the smallest grain size. In contrast, dual plateaus in impedance Bode plots were seen only for the microcrystalline sample. This behavior was successfully analyzed in terms of the brick-layer model (BLM), taking into account the contributions of the parallel grain boundaries. Simulation via the BLM model was performed as a function of ρ_{gb}, ρ_{gi}, ε_{gb}, ε_{gi}, D, and d. It was observed that the ratio of low frequency-to-high frequency capacitance goes through a maximum vs. grain size; the value of D/d (grain size-to-grain boundary width) at the capacitance maximum increases with the grain boundary-to-grain interior resistivity ratio (ρ_{gb}/ρ_{gi}). If D/d is less than ρ_{gb}/ρ_{gi}, there will be dual plateaus in both capacitance and impedance Bode plots (and a large grain boundary arc in the Nyquist plot); if D/d is greater than ρ_{gb}/ρ_{gi}, there will be two distinct plateaus in capacitance Bode plots only (and a small or negligible grain boundary arc in the Nyquist plot). The BLM was capable of generating all the observed features in experimental Nyquist and Bode plots of nano- and microcrystalline ceria. However, the other BLM fitting parameters (dielectric constant and width of grain boundaries) are problematic, being either too small (grain boundary width) or too large (grain boundary dielectric constant). This may suggest that the BLM is invalid or simply not representative of the actual microstructure in the specimens studied. What is certain is that the grain boundary resistivity in nanocrystalline specimens is significantly lower than in microcrystalline ceria, and closer in magnitude to that of the grain interiors.

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Notes

Since the original submission of this manuscript, Fleig and Maier have tackled the problem of simulating the impedance vs. frequency behavior of ''real'' ceramic microstructures via finite element analysis [21].

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